

DRAWINGS

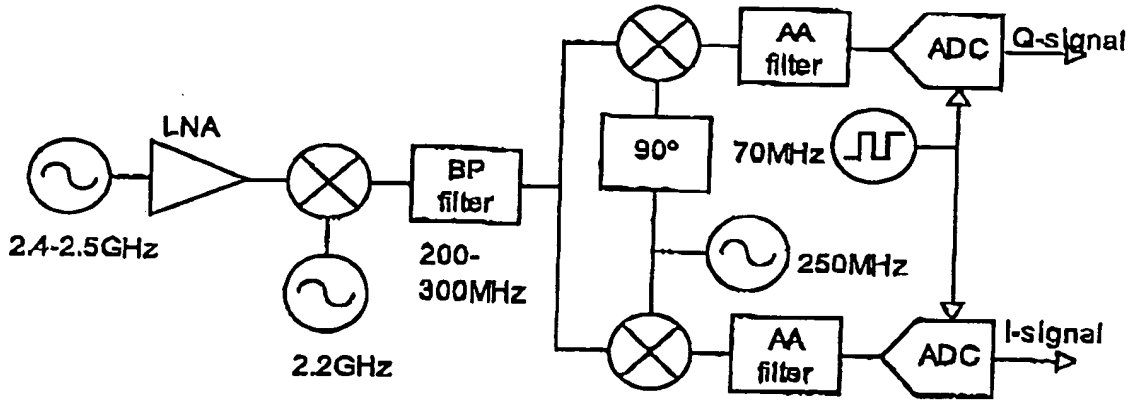


Figure 1

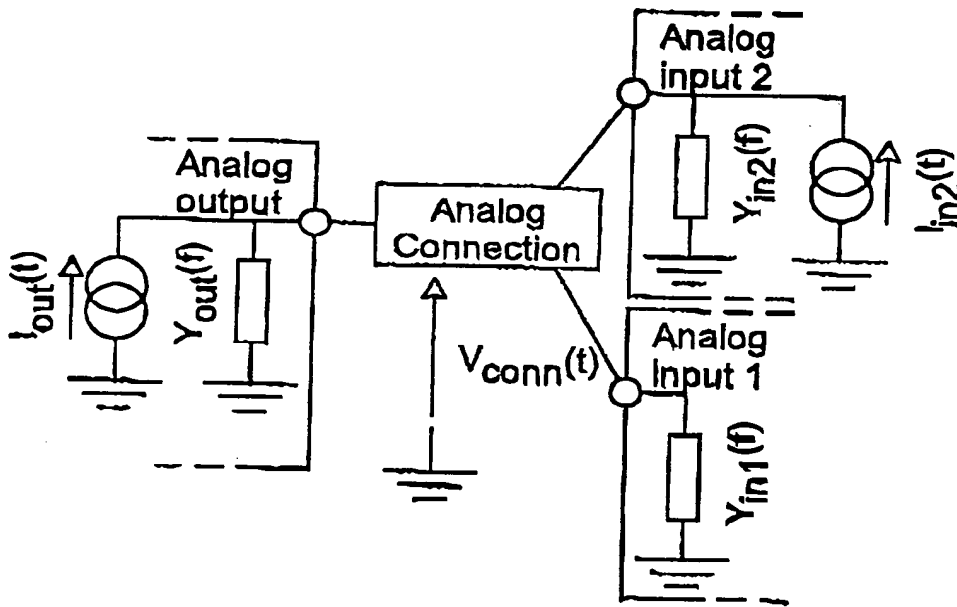
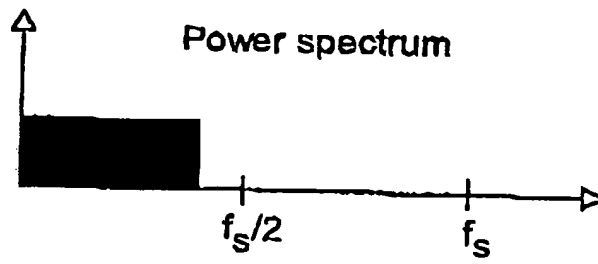


Figure 2

Baseband representation



Equivalent low-pass representation

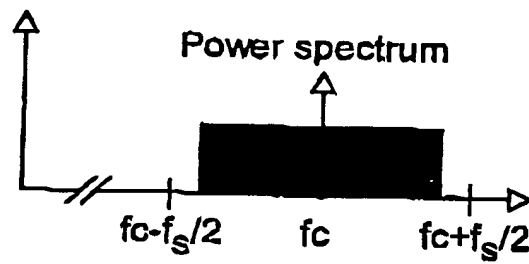


Figure 3

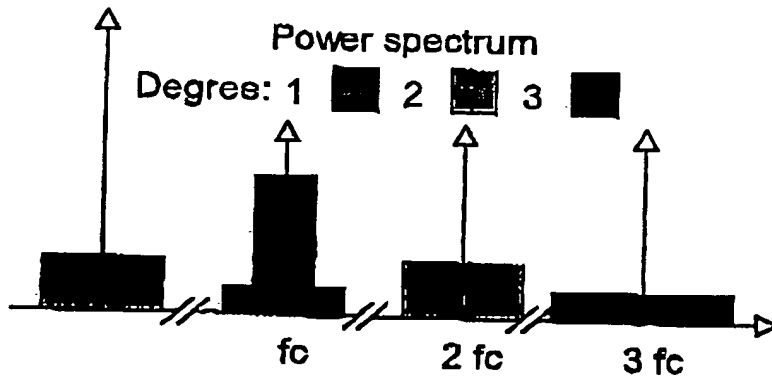


Figure 4

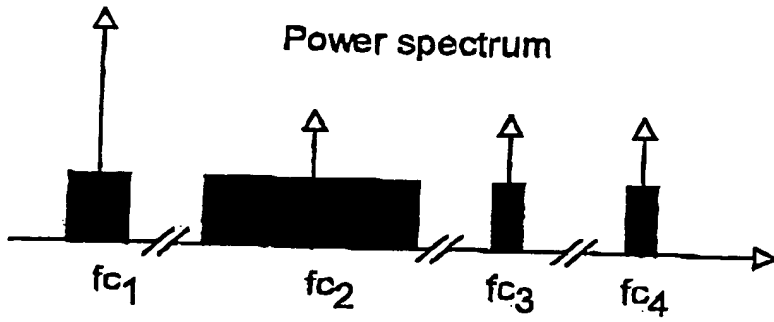


Figure 5

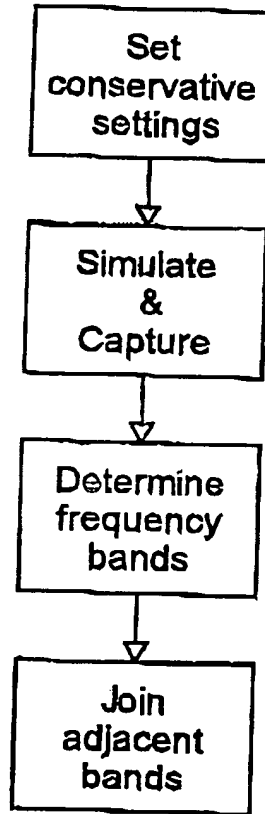


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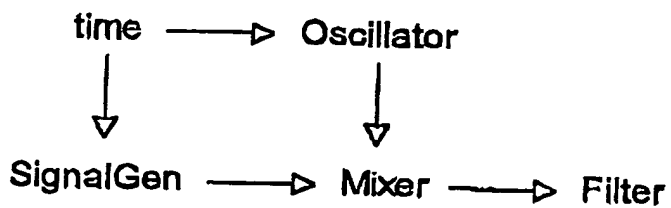
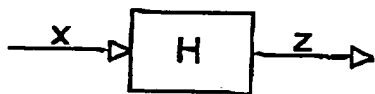
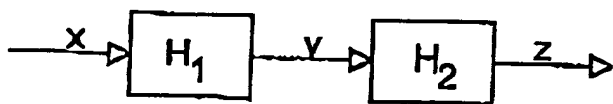


Figure 7



$H = \text{cascade}(H_1, H_2)$

Figure 8

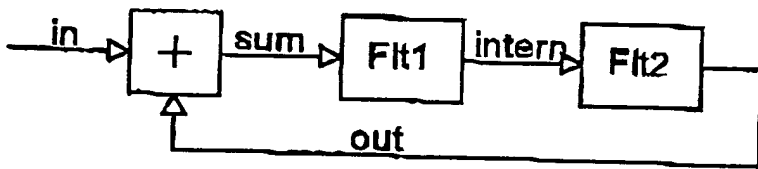


Figure 9

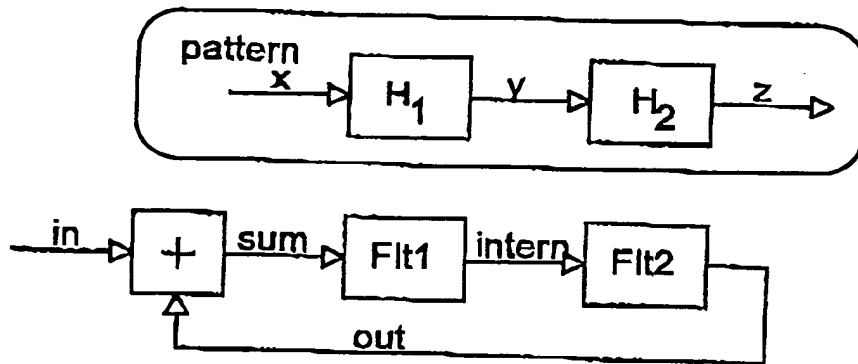


Figure 10

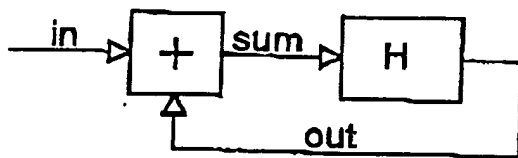


Figure 11

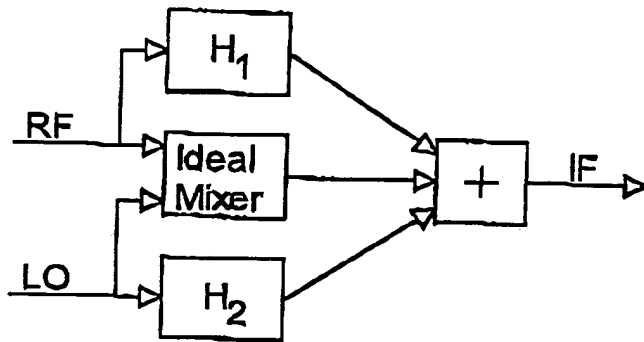


Figure 12

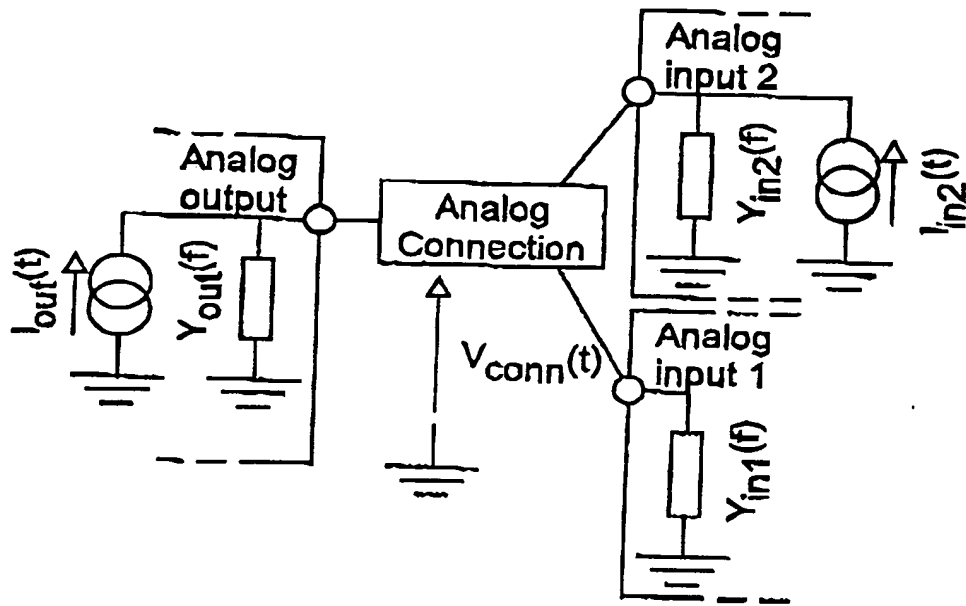


Figure 13

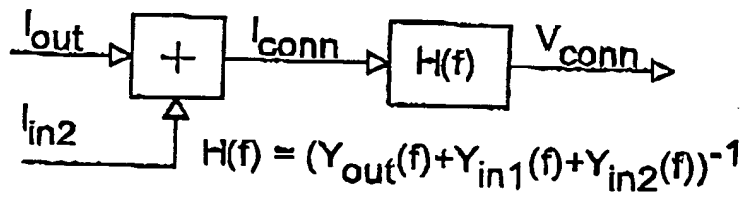


Figure 14

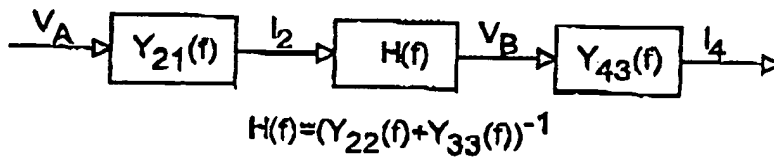
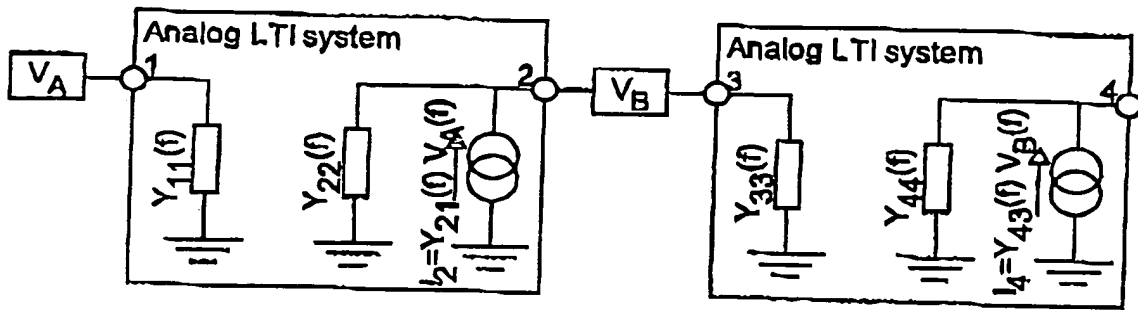


Figure 15

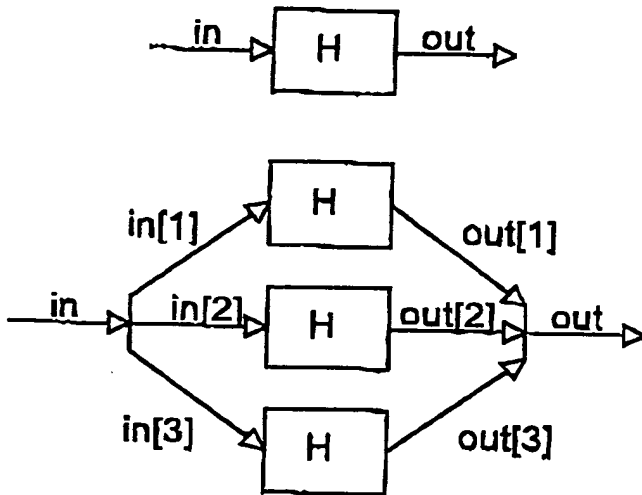


Figure 16

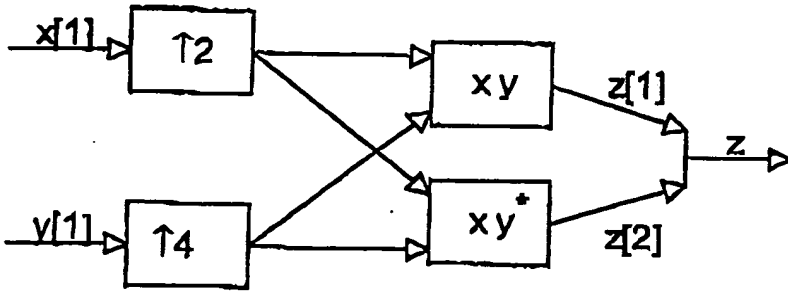
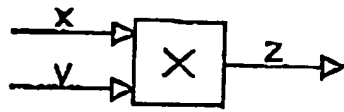


Figure 17

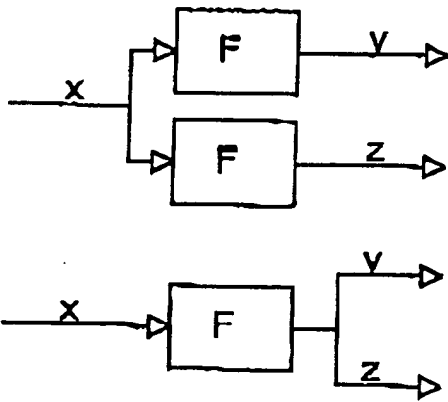


Figure 18

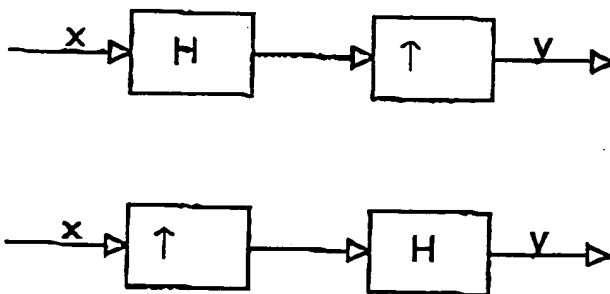
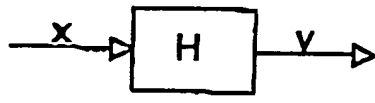
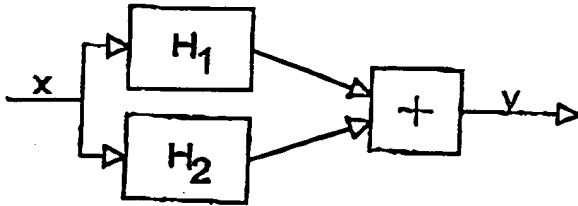
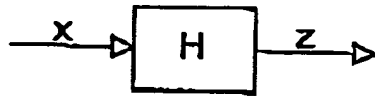
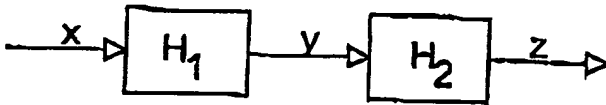


Figure 19



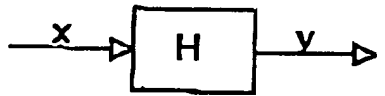
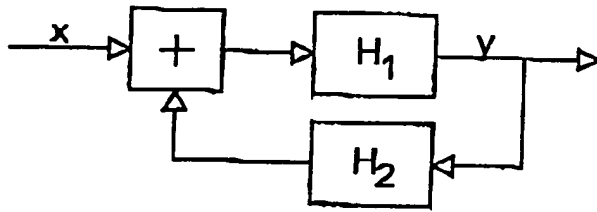
$$H = H_1 + H_2$$

Figure 20



$$H = \text{cascade } (H_1, H_2)$$

Figure 21



$$H = H_1 / (1 - H_1 H_2)$$

Figure 22

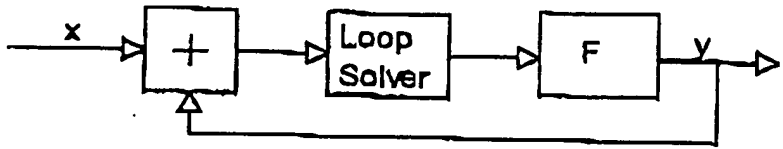
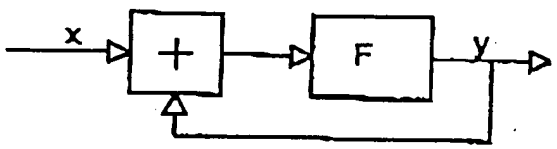


Figure 23

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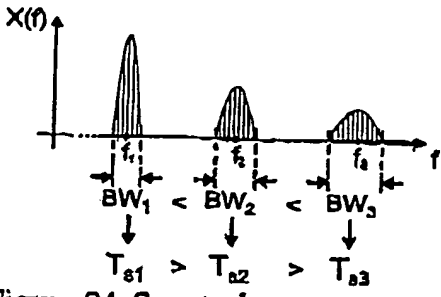


Figure 24: Spectral representation of an MPMC signal.

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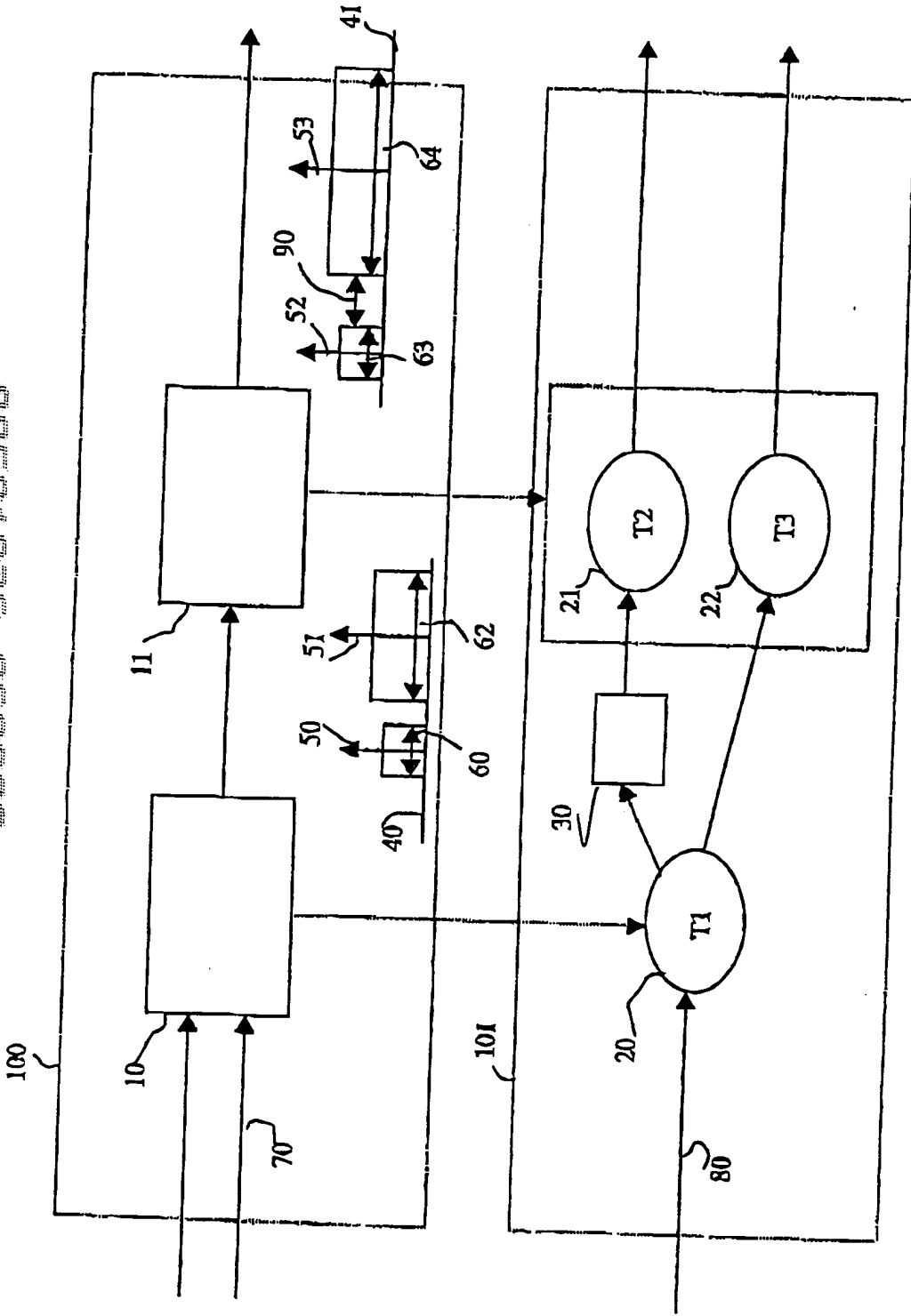


Figure 25

Figure 26

Figure 26 is a flowchart illustrating the steps of a simulation process. The steps are arranged vertically in a series of rectangular boxes. The steps are: 1. Input Circuit (graphical, text format), 2. Perform Preliminary Simulation, 3. Determine signal representations, 4. Simplify signal representations, 5. Construct Computational graph, 6. Add up/down sampling nodes, 7. Split linear subcircuits in plurality of nodes, 8. Determine computation method for nonlinear circuits, 9. Scheduling of computation nodes - preferring vector processing nodes, and 10. Executed Scheduled Computation Rules.

Input Circuit (graphical, text format)

Perform Preliminary Simulation

Determine signal representations

Simplify signal representations

Construct Computational graph

Add up/down sampling nodes

Split linear subcircuits
in plurality of nodes

Determine computation
method for nonlinear circuits

Scheduling of computation nodes - preferring vector processing nodes

Executed Scheduled Computation Rules

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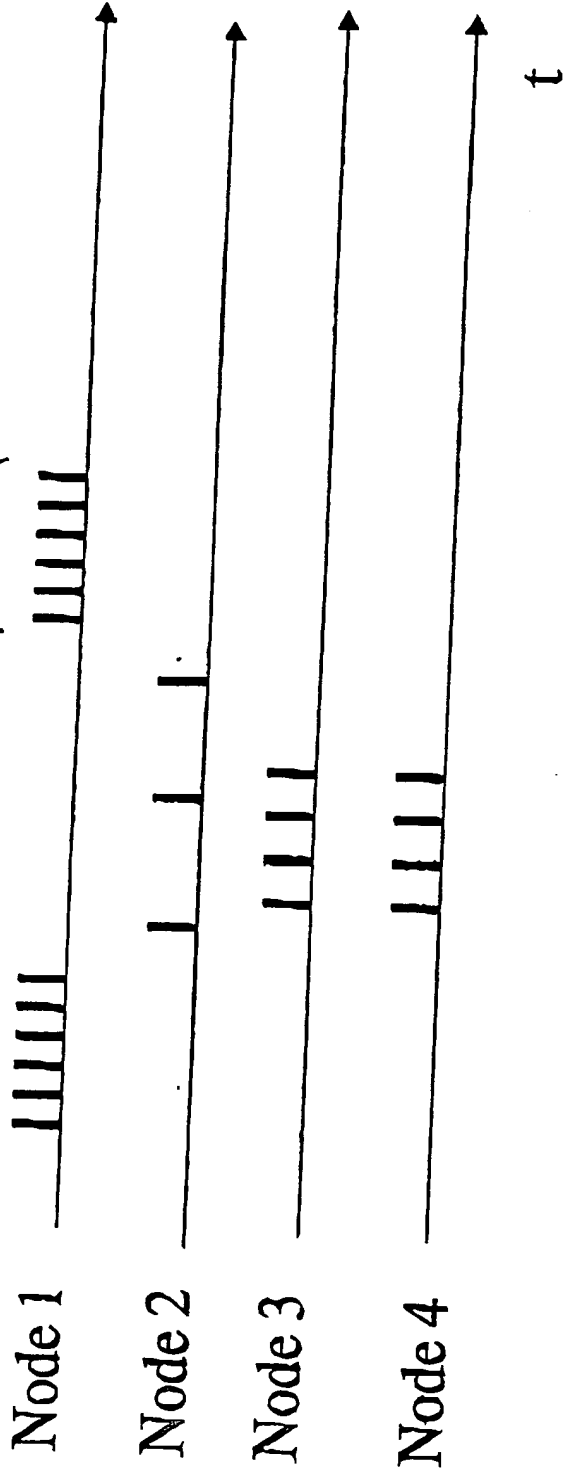


Figure 27